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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,379	09/17/2003	Darrin Benzer	13546US02	4562

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,379	BENZER ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 9-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kameyama et al. (USP 6,466,054) in view of Cress et al. (USP 6,483,386).

With respect to claims 9-15, 25 and 26, Figure 5 of the Kameyame et al. reference discloses a level shifter circuit (singled ended input circuit), which meets a method of translating a voltage level of a single-ended input signal (in) using at least one pass NMOS transistor device (801) having a gate that is constantly grounded (Col 4, lines 41-42), wherein the circuit includes: outputting a first voltage level if the single-ended input signal is in a first state (i.e., if the first state of the input signal "in" is at logic Lo, the output "out" of the circuit is at logic Hi; and if the first state of the input signal "in" is at logic Hi, the output "out" of the circuit is at logic Lo); and outputting a second voltage level if the single ended input is in a second state (i.e., if the first state of the input signal "in" is at logic Hi, the output "out" of the circuit is at logic Lo; and if the first state of the input signal "in" is at logic Lo, the output "out" of the circuit is at logic Hi). The Kameyama reference does not disclose that the at least one pass NMOS transistor device is a native NMOS transistor device having a threshold voltage less than 0V. However, the Cress et al. reference discloses (note M3 in Figure 5, lines 45-65 of Col. 2, lines 18-43 of Col. 3, and lines 4-31 of Col. 4 of Cress et al.) a pass transistor device (M3) is a native NMOS transistor device

having a threshold voltage less than 0V (-200mV, see lines 34-36 of Col. 3 of Cress et al.) for the purpose of having an input signal fully passes through the pass NMOS transistor device because the use of a native NMOS as a pass transistor provides a signal with low signal distortion (see line 24-31 of Col. 4, Cress et al.). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 5 of the Kameyama et al. reference by specifically using the native transistor having a threshold voltage of less than 0V, as taught by the Cress et al. reference, for the NMOS pass transistor (801) for the purpose of reducing noise and improving the performance of the circuitry since native NMOS pass transistor provides a signal with low distortion. Thus, this modification meets all the limitations of these claims including the limitation that the at least one native NMOS transistor device having a threshold voltage less than 0V (-200mV as discussed above).

With respect to claim 16, the above modification of the level shifter circuit as discussed above (with regard to claim 9) meets all the limitation of this claim, i.e., the modification circuit discloses a level shifter circuit, which meets a method of translating a voltage level of a single-ended input signal (in) using at least one native NMOS transistor device having a threshold voltage less than 0V (-200mv, see rejection of claim 9) including: determining if the input signal (in) is high (input signal "in" having logic Hi, n-channel transistor connected between "out" and Vss turns ON); outputting a low signal if the input signal is high (output signal "out" is a low signal if the input signal "in" is high); and outputting a high signal if the input signal is not high (p-channel transistor connected between "out" and Vdd is ON).

With respect to claim 17, the above modification meets the limitation that determining if the input signal is high includes determining if the input signal (in) is greater than a first voltage

(the threshold voltage of the n-channel transistor connected between "out" and Vss, i.e., the input signal "in" is considered to be Hi when the input signal "in" is greater than the threshold voltage of the n-channel transistor connected between "out" and Vss).

With respect to claim 18, the above modification meets the limitation that determining if the input signal (in) is not high includes determining if the input signal is less than a second voltage (the threshold voltage of the p-channel transistor connected between "out" and Vdd, i.e., the input signal in is considered to be Lo when the input signal in is less than the threshold voltage of the p-channel transistor connected between "out" and Vdd, so p-channel transistor connected between "out" and Vdd is ON).

With respect to claim 19, the above modification meets the limitation that eliminating static current drain (by the feedback transistor p-channel 802 in the above modification, i.e., when output "out" is Lo, then PMOS 802 is ON to cause the p-channel transistor connected between "out" and Vdd is OFF, so eliminate all static current drain. Note that this is similar as applicant's invention).

With respect to claims 20-24, the above modification (as discussed above with regard to claim 9) meets all the limitations of these claims, i.e., the level shifter circuit having a single-end input (in), a first native NMOS transistor (the replacement of the NMOS 801) having threshold voltage of less than 0V (-200mV, see discussion in claim 9), a second transistor (n-channel transistor connected between "out" and Vss), and a level shifter transistor (p-channel transistor connected between "out" and Vdd). Note that the method steps recited in this claim are also met including: determining if the input signal is greater than a threshold value of the second transistor (n-channel transistor connected between "out" and Vss turns ON if input signal "in" is greater

than threshold value of the n-channel transistor connected between "out" and Vss); outputting a low signal if the input signal is greater than the threshold value (n-channel transistor connected between "out" and Vss turns ON if input signal "in" is greater than threshold value of the n-channel transistor connected between "out" and Vss, so output "out" is Lo and having Vss voltage level); outputting a Hi signal if the input signal is not greater than the threshold value (if input signal "in" is not greater than threshold value of n-channel transistor connected between "out" and Vss, then p-channel transistor connected between "out" and Vdd turns ON so output "out" is Hi and having a VDD level); and eliminating static current drain (by feed back transistor PMOS 802, i.e., when output "out" is Lo, then PMOS 802 is ON to cause the p-channel transistor connected between "out" and Vdd is OFF, so eliminate all static current drain. Note that this is similar as applicant's invention); and wherein outputting a high signal comprising determining if the input signal is "greater" than a second threshold value (the threshold of p-channel transistor connected between "out" and Vdd because if the input "in" is greater than the threshold of p-channel transistor connected between "out" and Vdd, then the p-channel transistor connected between "out" and Vdd turns off; note that p-channel transistor connected between "out" and Vdd turns On when input signal "in" is less than the threshold of p-channel transistor connected between "out" and Vdd); and determining if the input signal is less than the threshold value but greater than the second threshold value (the output signal is not determined Hi or Lo).

3. Claims 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano (USP 5,650,742) in view of Cress et al. (USP 6,483,386).

Figure 12 of the Hirano reference discloses a level shifter circuit, which meets a method of translating a voltage level of a single-ended input signal (I12) using at least one pass NMOS

transistor device (either Qn1201 or Qn1204) including: outputting a first voltage level if the single-ended input signal is in a first state (i.e., if the first state of the input signal I12 is at logic Lo, the output O12 of the circuit is at logic Hi; and if the first state of the input signal I12 is at logic Hi, the output O12 of the circuit is at logic Lo); and outputting a second voltage level if the single ended input is in a second state (i.e., if the first state of the input signal I12 is at logic Hi, the output O12 of the circuit is at logic Lo; and if the first state of the input signal I12 is at logic Lo, the output O12 of the circuit is at logic Hi). The Hirano reference does not disclose that the at least one pass NMOS transistor device is a native NMOS transistor device having a threshold voltage less than 0V. However, the Cress et al. reference discloses (note M3 in Figure 5, lines 45-65 of Col. 2, lines 18-43 of Col. 3, and lines 4-31 of Col. 4 of Cress et al.) a pass transistor device (M3) is a native NMOS transistor device having a threshold voltage less than 0V (-200mV, see lines 34-36 of Col. 3 of Cress et al.) for the purpose of having an input signal fully passes through the pass NMOS transistor device because the use of a native NMOS as a pass transistor provides a signal with low signal distortion (see line 24-31 of Col. 4, Cress et al.). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 12 of the Hirano reference by specifically using the native NMOS pass transistor (M3) having a threshold voltage of less than 0V, as taught by the Cress et al. reference, for the NMOS pass transistor (Qn1201 and Qn1202) for the purpose of reducing noise and improving the performance of the circuitry since native NMOS pass transistor provides a signal with low distortion. Thus, this modification meets all the limitations of these claims including the limitation that the at least one native NMOS transistor device having a threshold voltage less than 0V (-200mV as discussed above). Thus, this modification/combination meets

all the limitations of claims 20-24, i.e., the level shifter circuit having a single-end input (I12), a first native NMOS transistor (the replacement of the Qn1201 and Qn1204 as discussed in claim 9) having threshold voltage of less than 0V (-200mV, see discussion in claim 9), a second transistor (Qn1202), and a level shifter transistor (Qp1202). Note that the method steps recited in this claim are also met including: determining if the input signal is greater than a threshold value of the second transistor (Qn1202 turns ON if input signal I12 than threshold value of Qn1202, respectively); outputting a low signal if the input signal is greater than the threshold value (Qn1202 turns ON if input signal I12 is greater than threshold value of Qn1202, so output O12 is Lo and having a ground voltage level); outputting a Hi signal if the input signal is not greater than the threshold value (if input signal I12 is not greater than threshold value of Qn1202, then Qp1202 turns ON so output O12 is Hi and having a VDD level); and eliminating static current drain (by feed back transistor Qp1201, i.e., when output "O12" is Lo, then PMOS Qp1201 is ON to cause the PMOS Qp1202 is OFF, so eliminate all static current drain); and wherein outputting a high signal comprising determining if the input signal is "greater" than a second threshold value (the threshold of Qp1202 because if the input I12 or I30 is greater than the threshold of Qp1202, then Qp1202 turns off; note that Qp1202 turns On when I12 is less than the threshold of Qp1202); and determining if the input signal is less than the threshold value but greater than the second threshold value (the output signal is not determined Hi or Lo).

Response to Arguments

4. Applicant's arguments filed on 5/16/06 have been considered but are moot in view of the new ground(s) of rejection as discussed above in the rejection.

Applicant also argues that "the examiner does not identify from Hirano or Cress any teaching of "eliminating static current drain of the level shifter". However, this argument is not persuasive because in the previous rejection, the examiner clearly identify in the combination/modification of Hirano and Cress that the step of "eliminating static current drain" is met by the feedback of transistor Qp1201. One skill in the art would understand the feedback of Qp1201 eliminates static current drain because when the input I12 is Hi, then Qp1202 turns ON so that output "O12" is Lo, then PMOS Qp1201 is ON to cause the p-channel transistor Qp1202 turn OFF so as to eliminate all static current drain.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG NGUYEN
PRIMARY EXAMINER